ISSN (Online): 2583-648X

IJIRID

International Journal of Ingenious Research, Invention and Development

An International, High Impact Factor, Double-Blind Peer-Reviewed, Open-Access, Multidisciplinary Online Journal

Volume 5 | Issue 4 | August 2026

www.ijirid.in

LFSR-Based Error-Resilient Ternary Content-Addressable Memory for High-Speed Fault-Tolerant Data Storage and Search

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Abstract: *Content-addressable memories provide fast parallel lookup but remain vulnerable to storage faults, synchronization errors, and implementation overhead when realized using SRAM-based structures. This work presents an Error-Resilient Ternary Content-Addressable Memory (ER-TCAM) that incorporates Linear Feedback Shift Registers (LFSRs) for randomized address generation and synchronized memory access. The proposed architecture combines LFSR-based storage, an address generation unit, a read/write controller, bit-wise error detection, and an Error Correction Vector (ECV) computation unit. The error-detection path generates an encoded indication of the faulty LFSR word, while the correction path reconstructs and rewrites the corresponding error-correction information without preventing lookup activity. The design was modeled in Verilog and implemented using Xilinx ISE 14.2. The supplied synthesis results report 32 slice registers, 128 LUTs, 16 fully used LUT-FF pairs, a delay of 0.316 ns, and power consumption of 0.042 W. The reported simulation also demonstrates recovery of an error-corrupted stored value to the correct output. Comparative results against DyTAN, MTCAM, and CN-TCAM show lower resource use, delay, and power for the proposed ER-TCAM.*

Keywords: TCAM, Content-Addressable Memory, Error Resilience, LFSR, FPGA, Soft Error, Error Detection, Error Correction, Verilog, Xilinx ISE.

I. Introduction

Modern digital systems require memories that can support both high storage density and rapid data retrieval. Conventional RAM accesses data by address, whereas a content-addressable memory (CAM) performs the inverse operation: the input is a data pattern and the memory returns the location of a matching entry. This characteristic makes CAM and TCAM structures attractive for high-speed search-oriented applications such as routing, lookup tables, pattern matching, data compression, coding, image processing, and signal-processing accelerators.

A ternary content-addressable memory extends binary comparison by supporting the three logical states 0, 1, and don't-care. This flexibility improves the efficiency of associative search, but the underlying memory cells and lookup structures remain sensitive to faults and transient errors. In SRAM-based realizations, an erroneous stored bit can alter the match result and thereby produce an incorrect lookup response. The source project therefore focuses on a fault-tolerant architecture that detects and corrects corrupted storage while preserving high-speed lookup.

The central idea is to combine an ER-TCAM organization with LFSR-based addressing. LFSRs generate pseudo-random address sequences using a compact network of flip-flops and XOR feedback. In the

 DOI: 10.5281/zenodo.22783123

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proposed design, the LFSR mechanism is used not only to accelerate and diversify address generation but also to support error identification and correction. The implementation objective is to reduce hardware resources, time delay, and power consumption while maintaining correct read/write and lookup behavior.

The main contributions reported in the supplied design are: (i) an ER-TCAM for fast read-write operations; (ii) LFSR modules for random pattern generation with address synchronization; and (iii) integrated self-error detection and correction within the LFSR-based TCAM structure.

II. Background and Related Work

2.1 CAM and TCAM Organization: A CAM is organized as an array of slots in which the stored word is compared in parallel with an external search key. A response register records the slots that match the comparand, and a priority encoder may be used when more than one slot matches. TCAM adds a mask-like don't-care state so that selected bit positions do not participate in the comparison. This capability is important when a stored rule represents a range or prefix rather than a single exact binary word.

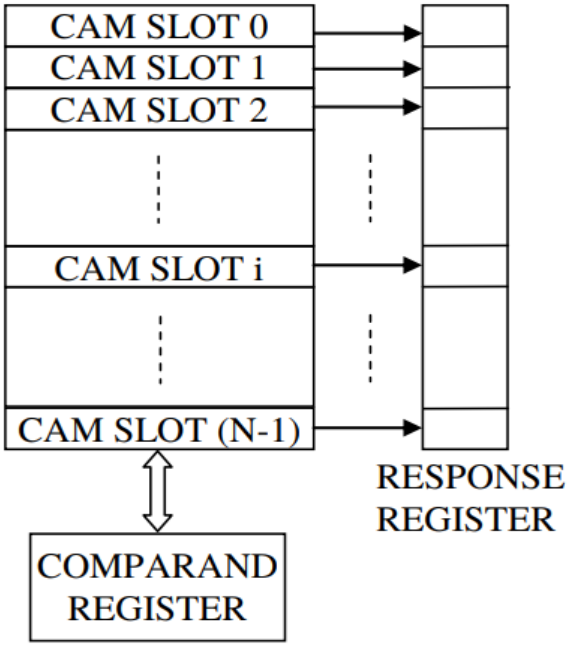

Figure 1: Basic TCAM organization with CAM slots, comparand register, and response register

2.2 Error-resilient TCAM Research: The literature summarized in the source project includes ferroelectric, MoS2, RRAM, spintronic, nanoelectromechanical, phase-change, FinFET, and FPGA-oriented TCAM implementations [1]-[25]. These studies target different combinations of search speed, non-volatility, power efficiency, compactness, and reliability. The source specifically compares the proposed implementation with DyTAN [22], a memristive TCAM (MTCAM) [23], and a compact nonvolatile TCAM (CN-TCAM) [24].

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The motivation for ER-TCAM is that soft errors in embedded SRAM structures can persist until the affected location is rewritten. A single corrupted memory word may therefore lead to a false match, a missed match, or an incorrect search result. The proposed method addresses this problem through concurrent error-detection and correction logic associated with the LFSR-based storage organization.

2.3 LFSR-based Address Generation: An LFSR is a sequential circuit constructed from flip-flops and XOR feedback. Its characteristic polynomial determines the feedback taps, while an initial seed determines the subsequent generated sequence. The source project uses the pseudo-random output sequence as a set of memory addresses. Unlike a conventional sequential counter that checks locations in fixed order, the LFSR introduces randomized access and can retain a previously successful address as the seed for a subsequent search.

The project also describes a configurable-width LFSR in which the active width depends on the terminal address used by the memory. A priority encoder selects the required feedback configuration, allowing address generation to be adapted to the currently occupied memory range rather than scanning unavailable locations.

III. Proposed LFSR-Based ER-TCAM Architecture

3.1 Error Detection Mechanism: The proposed error-detection path is shown in Fig. 2. When a lookup search key is applied, the read LFSR words are processed through bit-wise XOR logic to generate error indications. Error outputs from the participating LFSRs are encoded using an N-to-log2N encoder so that a damaged LFSR word can be uniquely identified. In parallel, bit-wise AND logic and match-information registers preserve the search result and the associated base-address information.

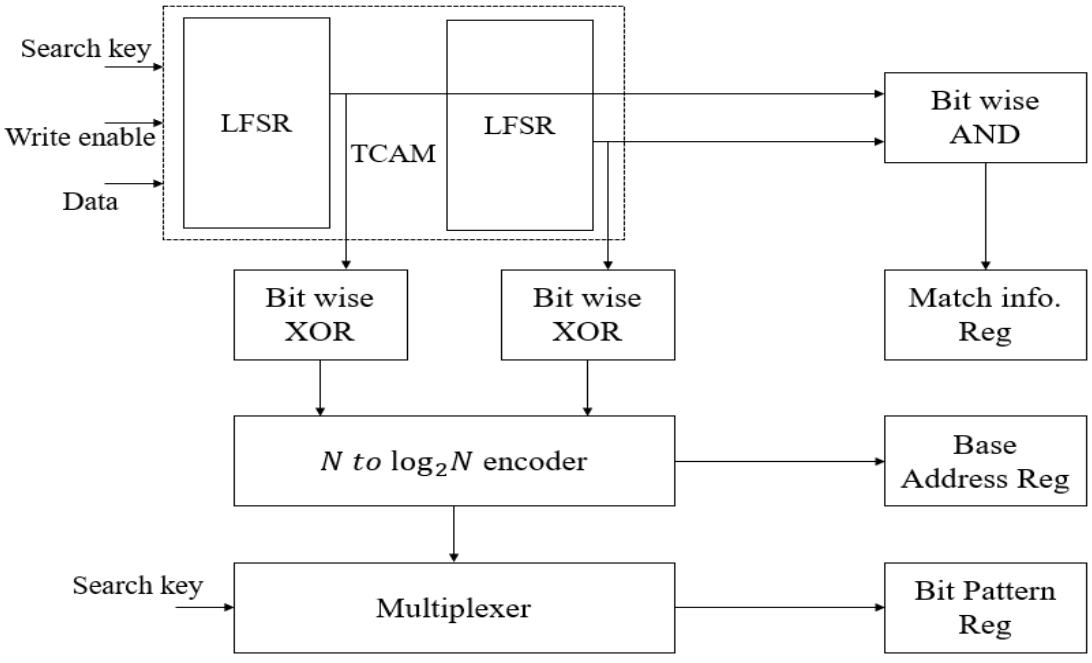

Figure 2: Error-detection mechanism of the proposed ER-TCAM

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3.2 Error Correction Architecture: The correction architecture contains an address-generation and read/write control unit, the LFSR-based TCAM table, and an ECV computation unit. The address-generation unit includes a MOD-D counter, an encoder, a comparator, and a multibit multiplexer. The lower address bits select words within a sub-block, while the encoded LFSR identifier selects the appropriate sub-block of the TCAM table.

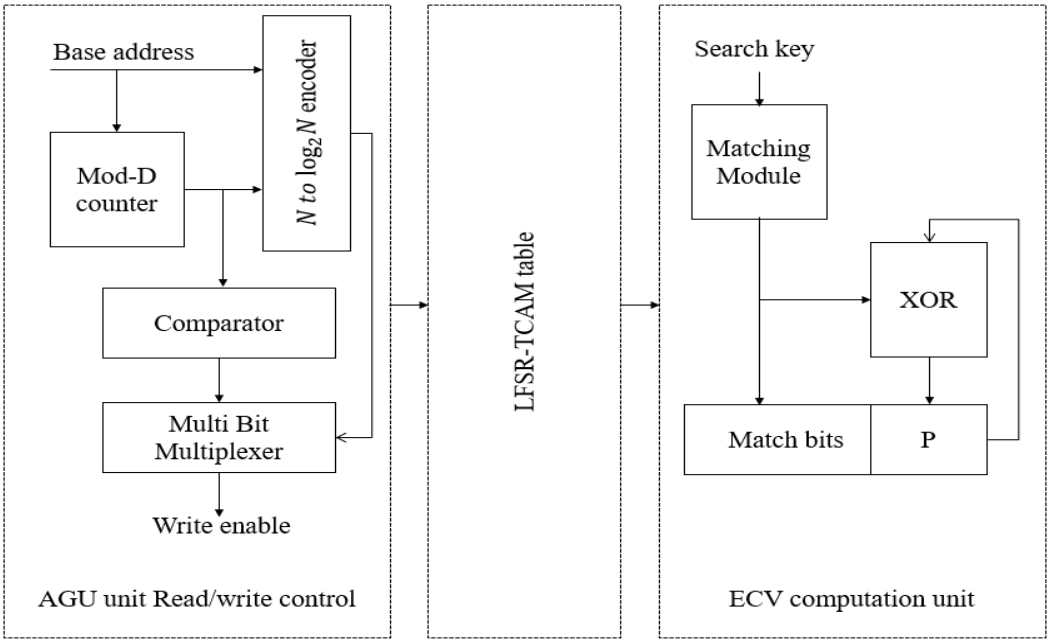

Figure 3: ER-TCAM error-correction architecture containing AGU/read-write control, LFSR-TCAM storage, and ECV computation

During correction, the selected TCAM words are compared with the search-key pattern to generate match bits. The match information and parity information together form the Error Correction Vector. Once the ECV has been obtained, the read/write controller asserts the write-enable signal for the relevant LFSR and rewrites the corrected information over the damaged word.

A key architectural property stated in the source is that search activity can continue while the error-correction process is active. The LFSR storage is treated as dual-port RAM so that the ECV can be written through one port while lookup proceeds through the other. Thus, the correction operation is designed to overlap with normal search operation rather than requiring the complete TCAM to be taken offline.

3.3 Read and Write Operation: During a write operation, input data is stored at the next available location and a terminal-address indication is updated. The terminal count is supplied to a priority encoder to determine the required LFSR width and activate the corresponding feedback taps. This prevents the address generator from repeatedly producing addresses outside the currently occupied memory region.

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For a read/search operation, the requested data is first latched internally. The LFSR is then activated and generates candidate addresses according to the encoded terminal count. Data read from each generated address is compared with the latched search value. When the values match, the search stops, the matching address is returned, and that address is retained as a seed for a subsequent search.

3.4 Controller Organization: The source design uses a finite-state controller with five states: Start, Write Data, Latch Data, LFSR Address Generation, and Output Address Generation. Control signals include Address Select, Data Compare Enable, and Compare Found. The controller selectively enables the address-selection and comparison blocks according to the current memory operation.

IV. FPGA Implementation Methodology

The proposed LFSR-based ER-TCAM was described in Verilog and implemented using Xilinx ISE 14.2. The evaluation includes device-utilization analysis, timing analysis, functional waveform simulation, and power analysis. The reported results are then compared against three TCAM implementations referenced in the source project.

Table 1: Implementation and evaluation setup reported in the source design

Implementation item	Reported setting / role
HDL	Verilog
Design environment	Xilinx ISE 14.2
Main memory structure	LFSR-based ER-TCAM
Key functional blocks	LFSR storage, AGU, read/write control, encoder, comparator, ECV computation
Evaluation outputs	Resource utilization, delay, simulation waveform, power
Comparison baselines	DyTAN [22], MTCAM [23], CN-TCAM [24]

V. Results and Discussion

5.1 FPGA Resource Utilization: The proposed implementation uses 32 slice registers and 128 LUTs. The report also lists 16 fully used LUT-FF pairs. These values indicate a compact FPGA realization relative to the comparison designs used in the source evaluation.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	32	35200	0%
Number of Slice LUTs	128	17600	0%
Number of fully used LUT-FF pairs	16	144	11%
Number of bonded IOBs	89	100	89%
Number of BUFG/BUFGCTRLs	1	32	3%

Figure 4: Xilinx device-utilization summary for the proposed ER-TCAM

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5.2 Timing Performance: The timing summary reports a total data-path delay of 0.316 ns. The source identifies this value as route delay for the analyzed path. The proposed value is lower than the reported delays of DyTAN, MTCAM, and CN-TCAM.

```
Data Path: data<13> to D1/dec_out_13
                                   Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   IBUF:I->O             9   0.000   0.316  data_13_IBUF (data_13_IBUF)
   LD:D                     -0.035          D1/dec_out_13
  ----------------------------------------
  Total                      0.316ns (0.000ns logic, 0.316ns route)
                                     (0.0% logic, 100.0% route)
```

Figure 5: Timing summary showing the reported 0.316 ns path delay

5.3 Error-injection simulation: The functional simulation provides a direct example of error detection and correction. A 16-bit value corresponding to 10 is written into the TCAM. An error value is introduced during storage, producing a corrupted stored result. After the error-detection and correction sequence, the output signal returns the correct value 10. This demonstrates the intended self-correcting behavior of the proposed architecture under the illustrated test case.

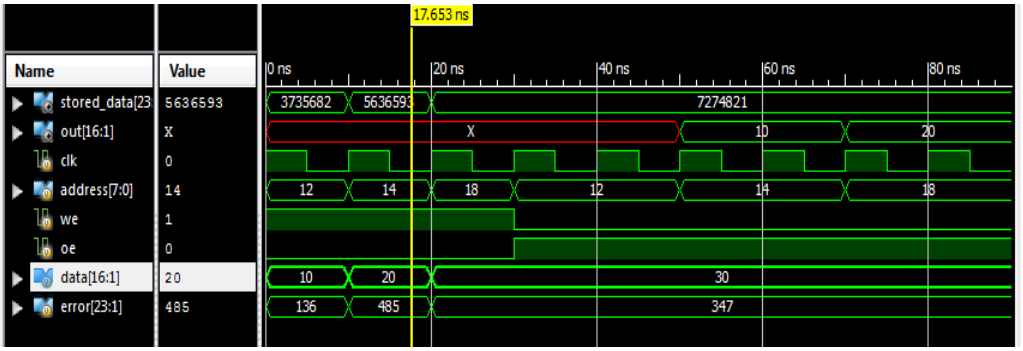

Figure 6: Simulation waveform demonstrating storage, injected error, and corrected output

5.4 Power Consumption: The Xilinx power report gives a power consumption of 0.042 W for the proposed ER-TCAM. This is the lowest value among the four designs in the supplied comparison table.

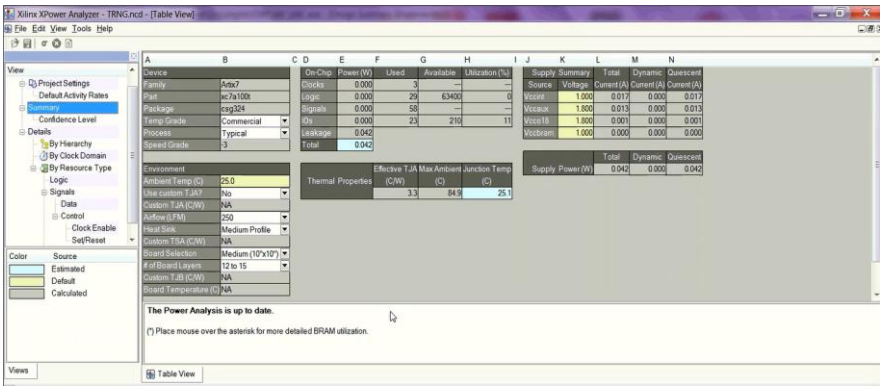

Figure 7: Power-analysis summary for the proposed ER-TCAM

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5.5 Comparative Evaluation:

Table 2: Performance comparison reported in the supplied document

Metric	DyTAN [22]	MTCAM [23]	CN-TCAM [24]	Proposed ER-TCAM
Slice Registers	125	78	46	32
LUTs	462	362	284	128
LUT-FFs	45	32	29	16
Time delay (ns)	0.927	0.837	0.735	0.316
Power (W)	0.826	0.734	0.386	0.042

Relative to DyTAN, the proposed ER-TCAM reduces the reported slice-register count by approximately 74.4%, LUT count by 72.3%, LUT-FF count by 64.4%, delay by 65.9%, and power by 94.9%. Relative to MTCAM, the corresponding reductions are approximately 59.0%, 64.6%, 50.0%, 62.2%, and 94.3%. Relative to CN-TCAM, the reported reductions are approximately 30.4%, 54.9%, 44.8%, 57.0%, and 89.1%, respectively. These percentages are directly derived from the numerical values in Table 2.

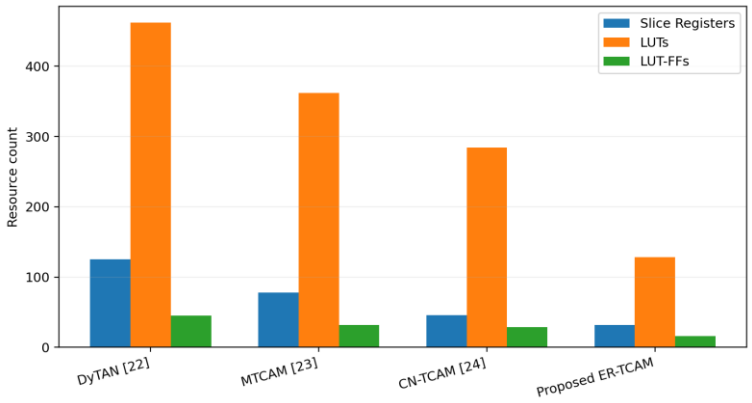

Figure 8: Resource-count comparison derived from the reported performance table

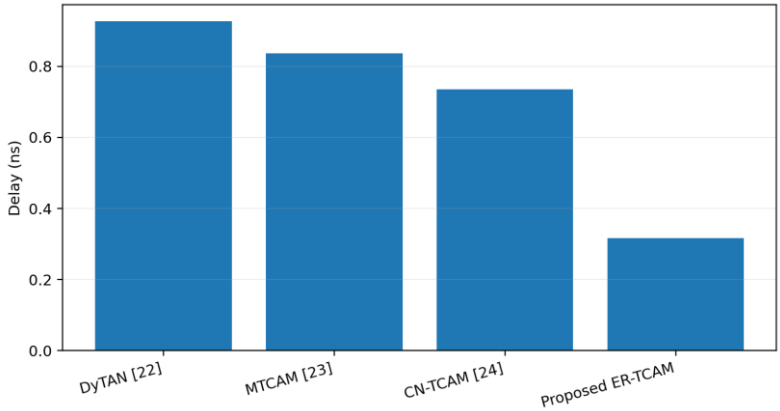

Figure 9: Delay comparison derived from the reported performance table

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International Journal of Ingenious Research, Invention and Development

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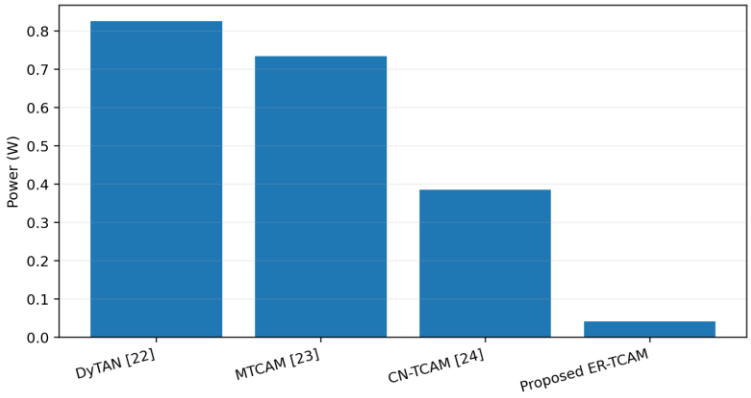

Figure 10: Power comparison derived from the reported performance table

5.6 Interpretation of Results: The reported improvements arise from combining compact LFSR address generation with an error-resilient TCAM organization rather than implementing a larger fault-handling structure around a conventional memory. The reduction in LUT and register counts is particularly important for FPGA-based systems because it leaves more programmable resources available for surrounding processing logic.

The simulation result is also important because resource and timing reductions alone do not establish fault tolerance. The waveform demonstrates that the design can identify an error-corrupted stored value and return the intended output after correction. In the architecture, this correction is intended to occur while search capability remains available through the dual-port organization.

VI. Advantages, Limitations, and Design Considerations

Table 3: Summary of architectural strengths and evaluation scope

Aspect	Observation from the proposed design
Search organization	TCAM-style content lookup with LFSR-based address generation
Fault handling	Built-in error detection and ECV-based correction
Concurrency	Search is intended to continue while correction is written through a separate port
Area	32 slice registers, 128 LUTs, and 16 LUT-FF pairs in the reported implementation
Timing	0.316 ns reported path delay
Power	0.042 W reported by the power analysis
Implementation scope	Results are FPGA/Xilinx-tool results from the supplied design; no fabricated-silicon measurements are provided

The supplied work demonstrates the ER-TCAM concept at the HDL/FPGA evaluation level. It does not provide fabricated-silicon measurements, process-voltage-temperature characterization, radiation

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testing, or a statistical fault-injection campaign. Therefore, the numerical results in this manuscript should be interpreted as implementation and simulation results from the reported Xilinx design environment rather than as silicon measurement results.

VII. Future Work

A natural extension of the reported work is to replicate multiple ER-TCAM modules for parallel memory allocation and search. The source conclusion explicitly identifies parallel LFSR-based ER-TCAM allocation as a direction for improved performance. Additional future evaluation could also increase the number and types of injected storage errors and quantify correction behavior across larger TCAM configurations, while retaining the same architectural principles used in the current implementation.

VIII. Conclusion

This paper has presented an LFSR-based Error-Resilient Ternary Content-Addressable Memory designed for fast data storage, high-speed lookup, and self-error recovery. The architecture uses randomized LFSR address generation, encoded error identification, an address-generation/read-write controller, and Error Correction Vector computation. The correction mechanism is organized so that the affected LFSR word can be rewritten while lookup activity remains available through the dual-port memory organization.

The supplied Xilinx ISE 14.2 implementation reports 32 slice registers, 128 LUTs, 16 LUT-FF pairs, a delay of 0.316 ns, and power consumption of 0.042 W. The simulation demonstrates recovery of a corrupted stored value to the correct output. Based on the comparison data provided in the source project, the proposed ER-TCAM achieves lower area-related resource counts, lower delay, and lower power than DyTAN, MTCAM, and CN-TCAM. These results support the use of LFSR-assisted error-resilient TCAM structures for FPGA-based high-speed associative-memory applications.

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